Amendments to the Specification: Please amend the specification as follows:

Please replace paragraph **[0064]** with the following amended paragraph **[0064]**.

[0064] The device shown in Figure 4D is fabricated by forming the P wells 492 and 493 in the N- substrate 110" and then forming the N+ diffusions 490 and 495 as well as the source and drain N+ diffusions for the transistors 496, 497 and 498. Next, the gate oxide layer 101 is deposited and the polysilicon electrodes 104 and 104' are formed on top of the gate oxide layer. If the gap-stabilizing implant ~~466~~ 494 is used, it is implanted as a self-aligned N-- implant through the gap between the electrodes 104 and 104'. This implant may be, for example, an optional threshold adjusting implant in the CMOS process. If the gap is stabilized using the electrode 310, then the next step is to form the oxide layer 312 over the polysilicon gate electrodes 104 and 104'. The step of depositing the metal electrode 310 also forms the metal connections to the blooming drain 490, to the charge sink 495 and to the transistors 496, 497 and 498. In the exemplary embodiment of the invention, these metal gates and connections are formed from a refractory metal such as copper. After this structure is formed, the wafer is thinned by removing the section 482 of the N- substrate 110". After the thinning operation, the structure shown in Fig. 4D is annealed at high temperature, for example, 900 degrees Celsius. As shown in Fig. 4D, the exemplary image may include an optional N+ diffusion 483 which is formed after the wafer is thinned but before it is annealed.